Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **V+ REF**
2. **V- REF**
3. **V+ HEATER**
4. **V- GND/ SUBSTRATE**

**4 1**

**3**

**2**

**DIE ID**

**NOTE: Chip back must be connected to Gnd**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .053” X .055” DATE: 9/12/16**

**MFG: NATIONAL THICKNESS .012” P/N: LM199**

**DG 10.1.2**

#### Rev B, 7/1